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In the Specification

Beginning on page 7, line 10, please insert the following paragraphs:

FIG. 9A is a model of the NOR gate shown in FIGS. 7A and 7B, wherein the model has been generated by summing the widths of the PFETs and NFETs into a single PFET and a single NFET.

FIG. 9B is a model of the NOR gate shown in FIGS. 7A and 7B, wherein the model is generated by choosing the sum of the widths of the PFETs receiving input B (of NOR gate 163) and the sum of the widths of the NFETs receiving input B.